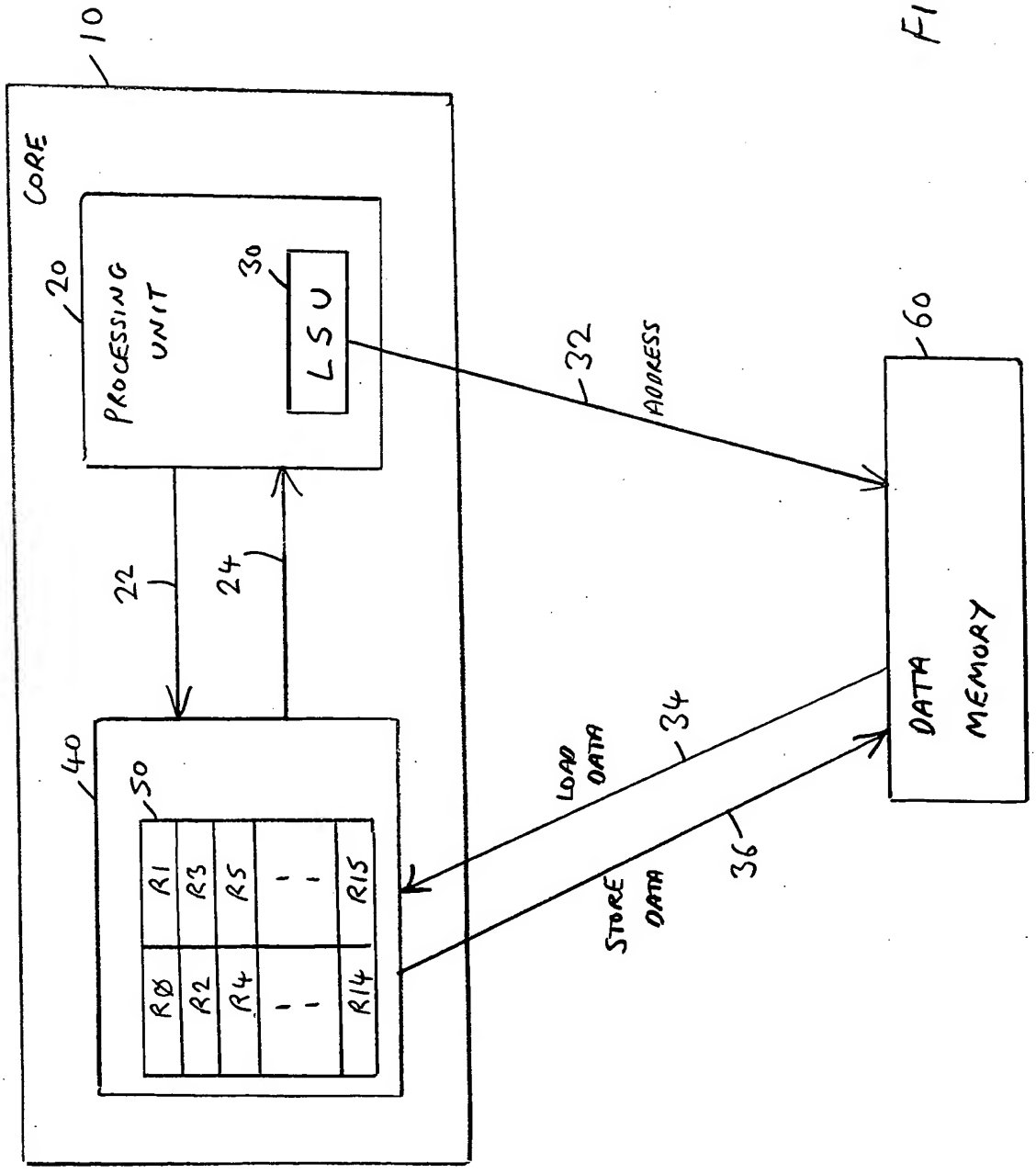
10
CORE
20
PROCESSING UNIT
30
LSU
32
ADDRESS
60
22
24
40
50
R0
R1
R2
R3
R4
R5
R14
R15
LOAD DATA
34
STORE DATA
36
DATA MEMORY

FIG. 1

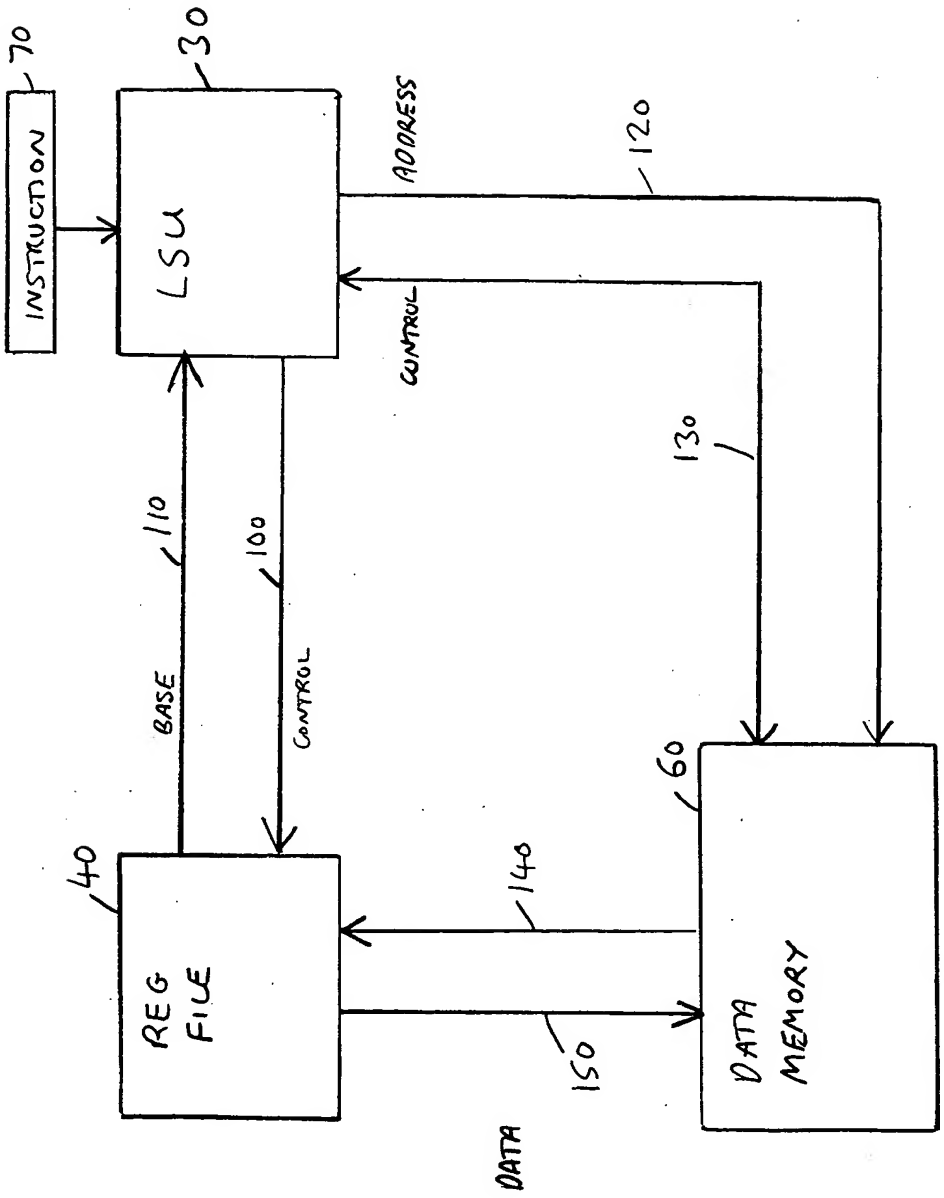
70
INSTRUCTION
30
LSU
ADDRESS
120
CONTROL
130
110
100
BASE
CONTROL
60
40
REG FILE
140
150
DATA MEMORY
DATA

FIG. 2

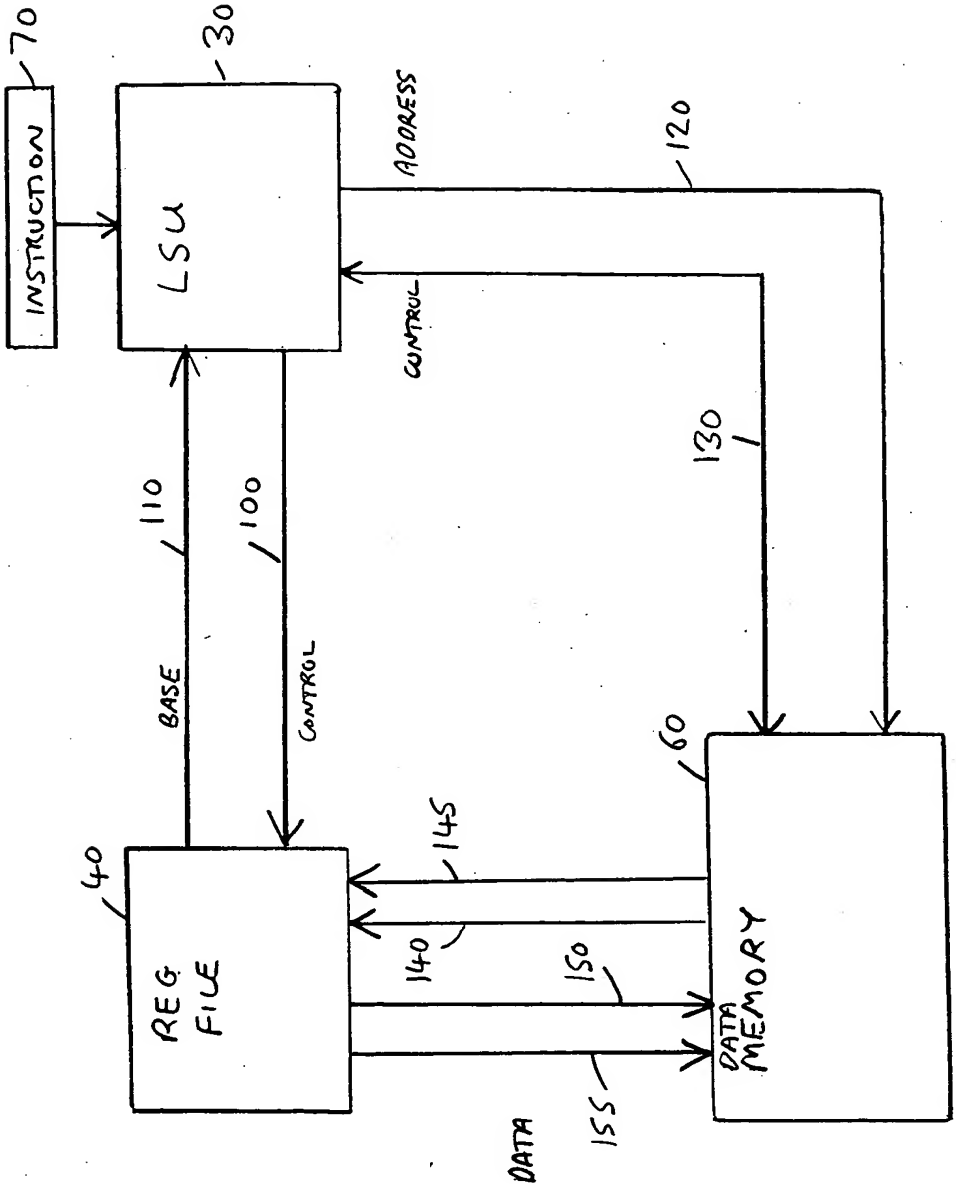
70
INSTRUCTION
30
LSU
ADDRESS
120
CONTROL
130
110
BASE
100
CONTROL
60
145
40
REG FILE
140
150
DATA MEMORY
155
DATA

FIG. 3

$LDRD_{NEW}$ R_x, R_y, [R_z, #offset]

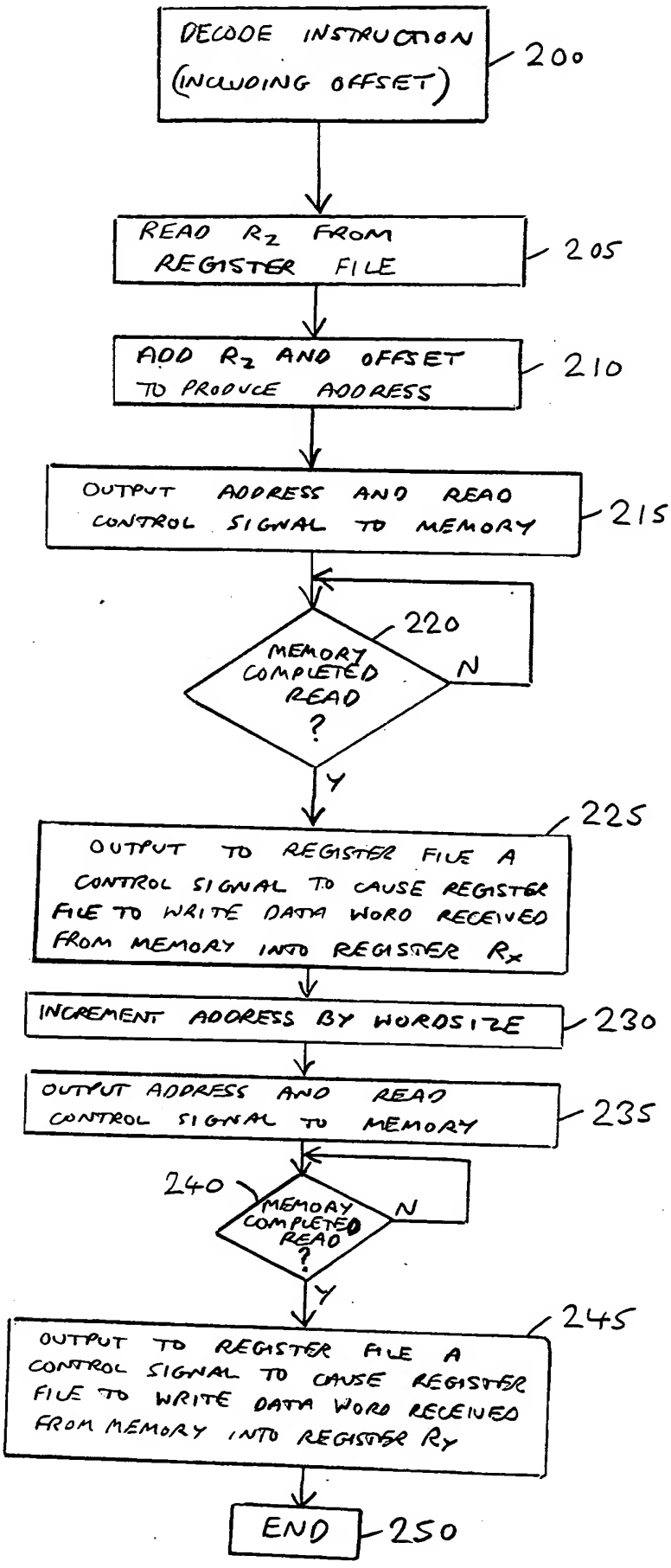

FIG. 4

$LDRD_{NEW}$ R_x, R_y, [R_z, #offset]

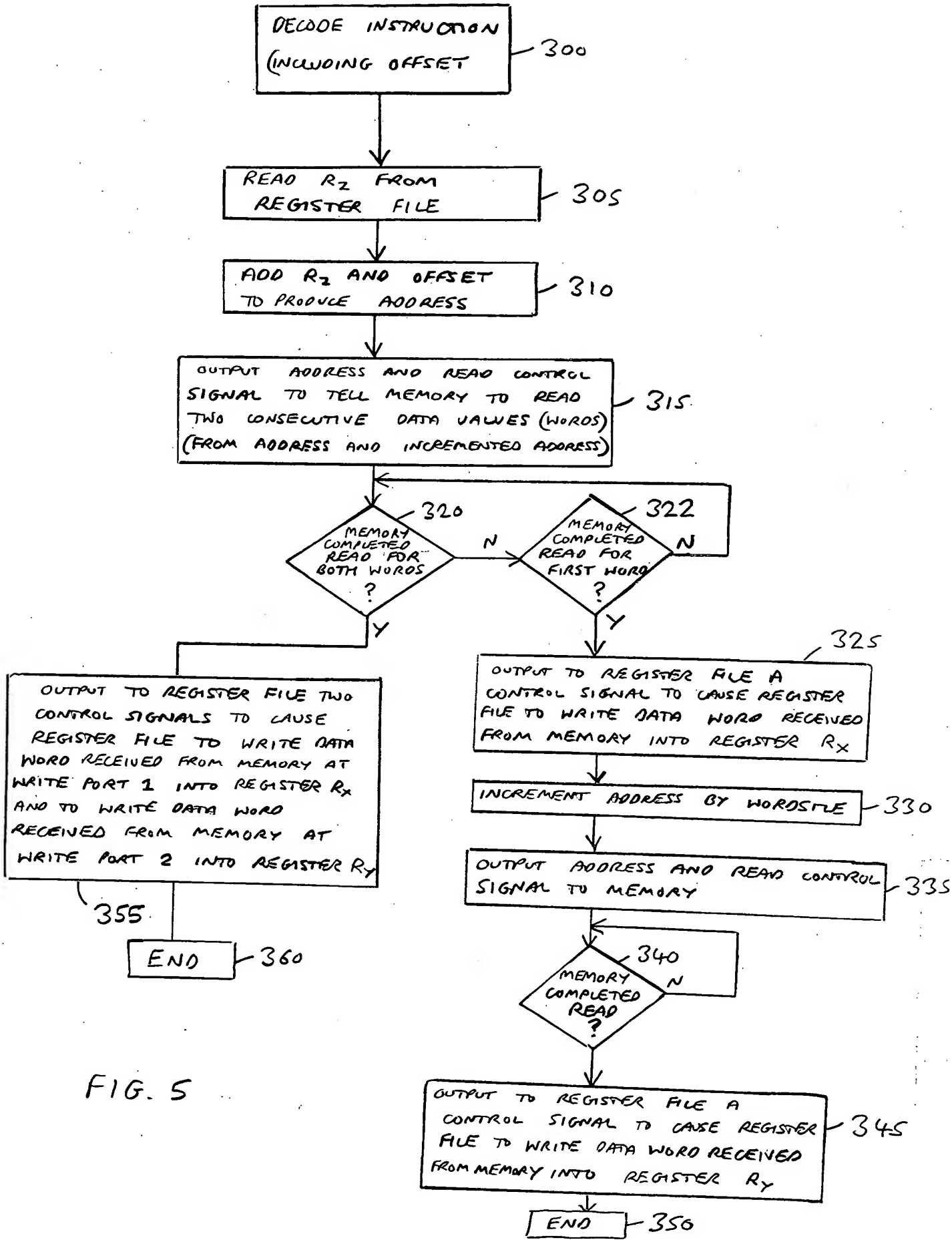

FIG. 5

STRD.NEW R_x, R_y, [R_z, # OFFSET]

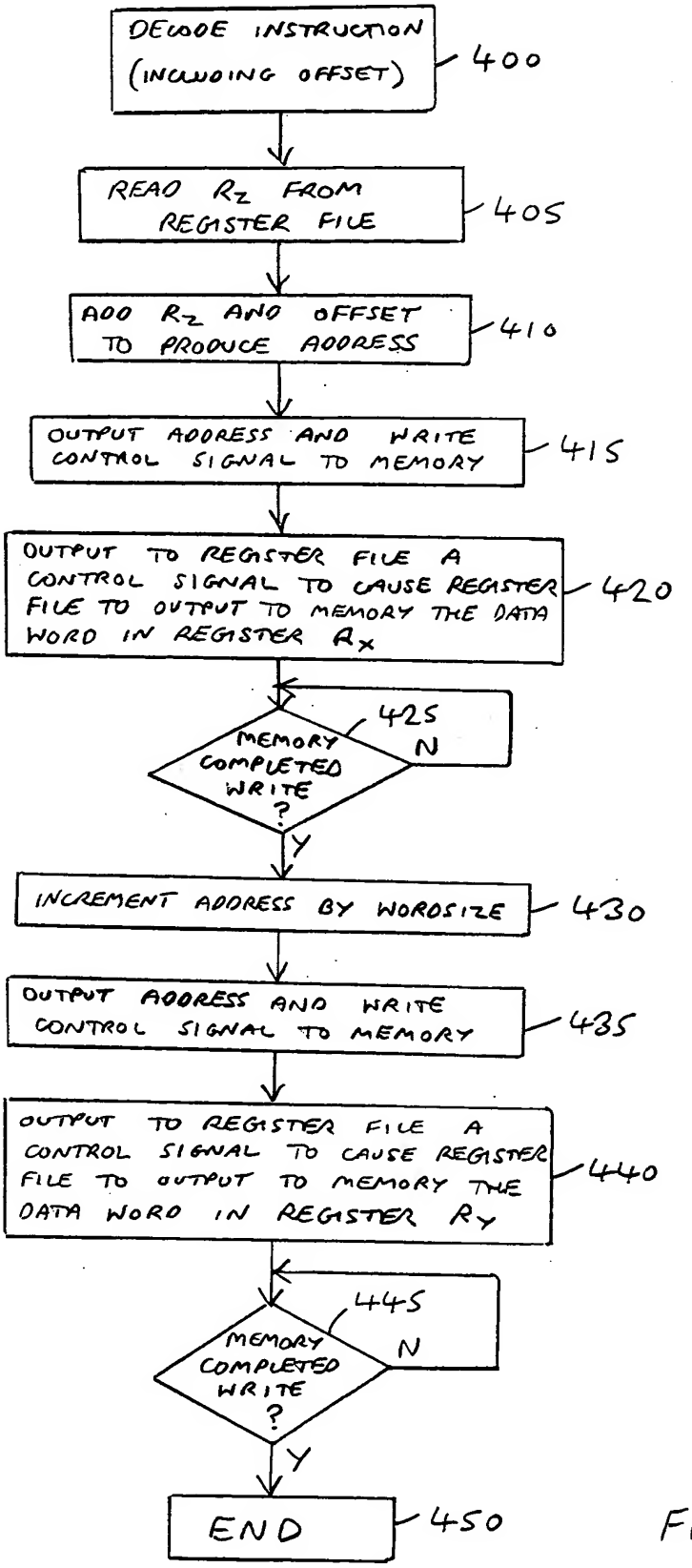

FIG. 6

STRD$_{NEW}$ R_x, R_y, [R_z, #OFFSET]

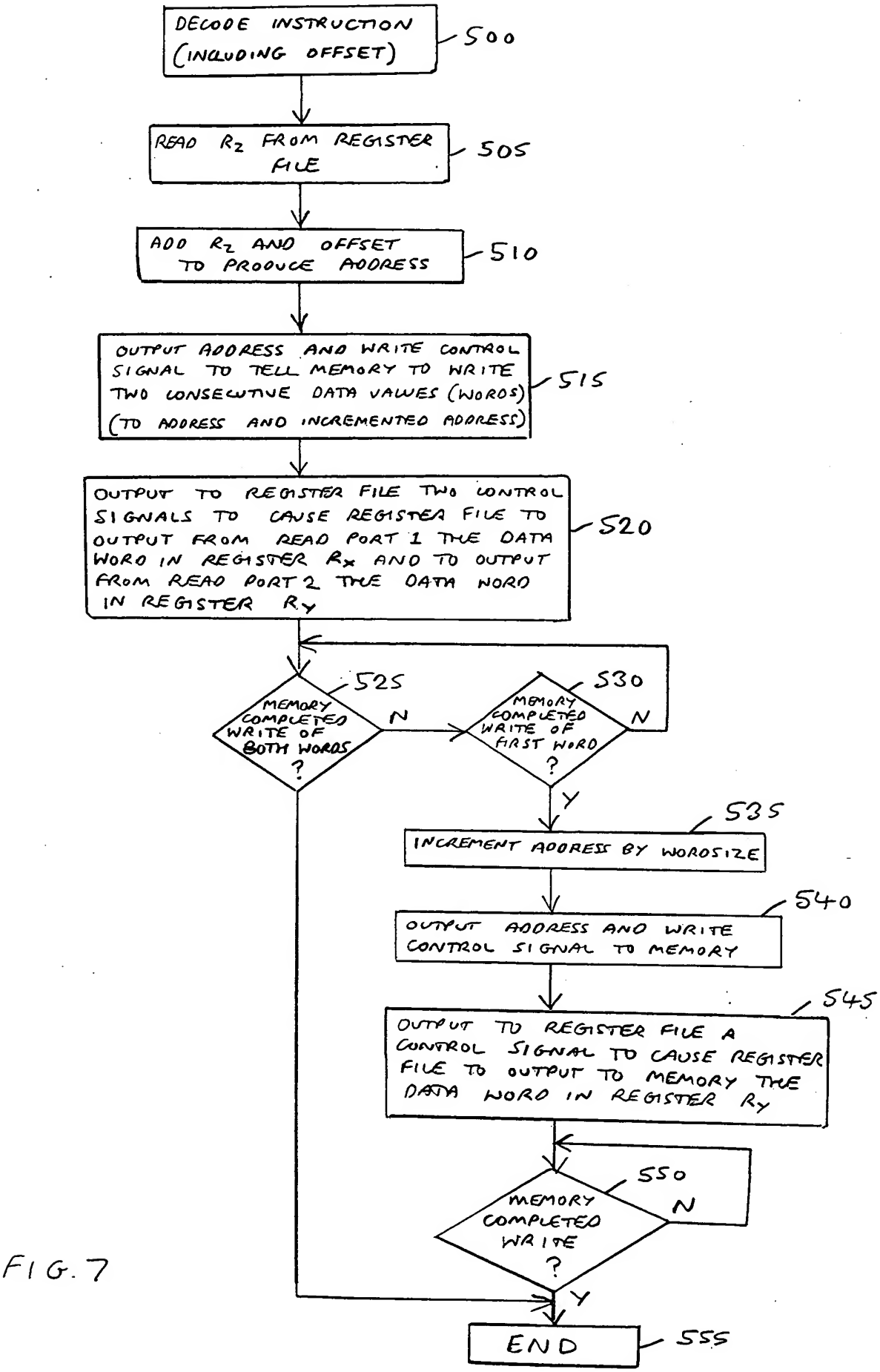

FIG. 7

```
LOR   RØ , [R4, #0]      LDMIA   R4, { RØ, R1 }
LOR   R1 , [R4, #4]      LDRD    RØ , [ R4, #0]
                         LDRD_NEW   RØ, R1, [R4, #0]
```

FIG. 8A

```
LOR   RØ , [R4, #8]      X  LDMIA
LOR   R1 , [R4, #12]     LDRD    RØ, [R4, #8]
                         LDRD_NEW  RØ, R1, [R4, #8]
```

FIG 8B

```
LOR   RØ, [R4, #0]       LDMIA   R4 , { RØ, R2 }
LOR   R2, [R4, #4]       X  LDRD
                         LDRD_NEW   RØ, R2, [ R4, #0]
```

FIG 8C

```
LOR   R2, [R4, #4]       X  LDMIA
LOR   RØ, [R4, #8]       X  LDRD
                         LDRD_NEW   R2,RØ, [R4, #4]
```

FIG. 8D

```
LOR   RØ, [R4 , #12]     X  LDMIA
LOR   R1 [R4 , #16]      X  LDRD
                         LDRD_NEW   RØ, R1, [R4, #12]
```

FIG 8E

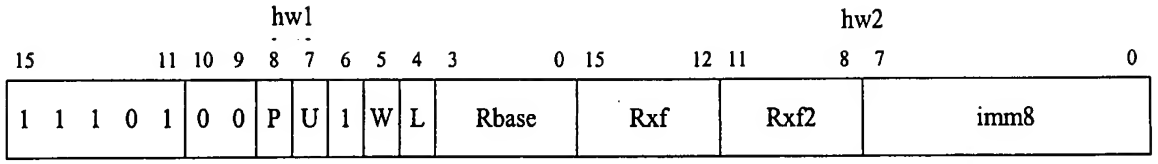
hw1
hw2
15 11 10 9 8 7 6 5 4 3 0 15 12 11 8 7 0
1 1 1 0 1
0 0
P
U
1
W
L
Rbase
Rxf
Rxf2
imm8

FIGURE 9